

Architecture des ordinateurs 2

Cours 8 - Timer

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Janvier 2018

Timer

- Éviter les attentes actives

Le Timer 0

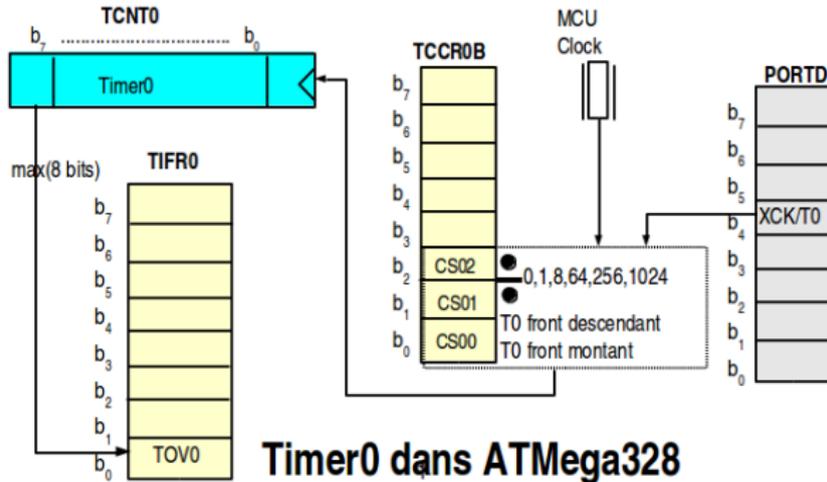


FIGURE – Le Timer 0

Prescaler

Table 19-10. Clock Select Bit Description

CA02	CA01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	$\text{clk}_{I/O}/1$ (No prescaling)
0	1	0	$\text{clk}_{I/O}/8$ (From prescaler)
0	1	1	$\text{clk}_{I/O}/64$ (From prescaler)
1	0	0	$\text{clk}_{I/O}/256$ (From prescaler)
1	0	1	$\text{clk}_{I/O}/1024$ (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

If external pin modes are used for the Timer/Counter0, transitions on the T0 pin will clock the counter even if the pin is configured as an output. This feature allows software control of the counting.

FIGURE – Select Bit

Prescaler registre TCCR0

Name: TCCR0B

Offset: 0x45

Reset: 0x00

Property: When addressing as I/O Register: address offset is 0x25

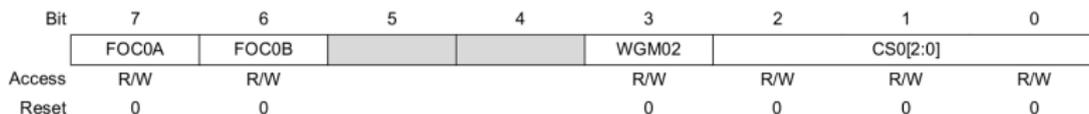


FIGURE – TCCR0B

- Le registre TCCR0 gère le prescaler à l'aide de trois bits CS2, CS01, CS00

Timer 8bits

Name: TCNT0

Offset: 0x46

Reset: 0x00

Property: When addressing as I/O Register: address offset is 0x26

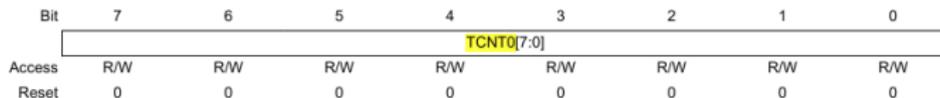


FIGURE – TCNT0

Timer overflow

Name: TIFR0

Offset: 0x35

Reset: 0x00

Property: When addressing as I/O Register: address offset is 0x15



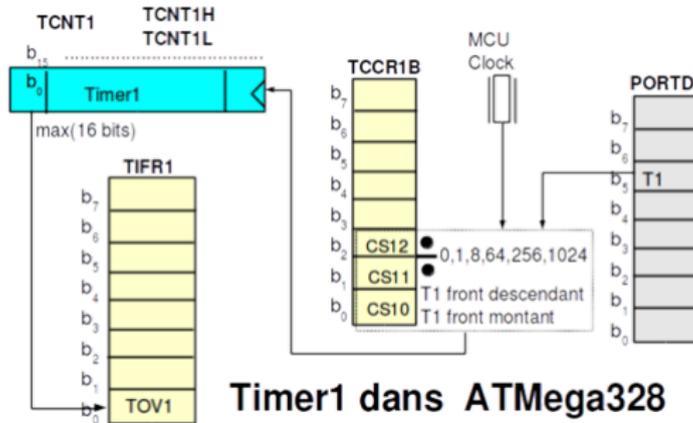
FIGURE – TIFR0

- Un bit d'un registre TIFR est appelé TOV0 (Timer overflow 0 = débordement du timer 0). Ce bit est automatiquement positionné à 1 lors du débordement du timer 0, c'est-à-dire pour un passage de 0xFF à 0x00.

Blink

```
int main(void){
    TCCR0 = 0x02; // prescaler 8
    TCNT0 = 0x00; // tmr0
    DDRB |= 0x01; //RB0
    while(1) {
        while ((TIFR & (1<<TOV0)) == 0);
        PORTB ^= 0x01;
        TIFR |= 0x01;
        // TIFR |= (1<<TOV0);
    }
    return 0;
}
```

Le Timer 1



Timer1 dans ATmega328

FIGURE – Le Timer 1